UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,337	12/26/2001	Steven K. Hsu	42390.P12624	1975

7590 08/06/2003

Seth Z. Kalson
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER
YOHA, CONNIE C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,337	HSU ET AL.	
	Examiner	Art Unit	
	Connie c. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 7-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *3-4, 16-17,20-21* is/are allowed.

6)☐ Claim(s) *1,7-15,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Examiner took notice of the remarks and amendments made by applicant filed on 5/12/03.

2. A second non-final rejection is applied to the pending claims using newly cited reference.

Response to Amendment

3. This office action is in response to Amendment filed on 1/4/00.

Claim 1, 3, 8-10, 12-14, 16-21 are amended.

Claims 2, 5, 6 are canceled.

4. Claims 1, 3, 4, 7-21 are pending.

Claim Rejections - 35 USC § 112

5. Claim 8-15 and 18-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the limitations.

In claim 8, recite the limitation "a read operation", in line 4.

In claim 9, recite the limitation "a read operation" in line 2 and 5; "an evaluation phase" in line 3 and 5; "a pre-charge phase", in line 4-5;

"a read-select transistor", in line 5.

In claim 10, recite the limitation "a read operation", in line 2 and 5-6;

"an evaluation phase", in line 3 and 5; "a pre-charge phase", in line 4-5.

In claim 11, recite the limitation: "a foot transistor", in line 12.

In claim 12, recite the limitation "a read operation" in line 8.

In claim 13, recite the limitation "a read operation" in line 2; "an evaluation phase" in line 3 and 5; "a pre-charge phase", in line 4-5;

"a read-select transistor", in line 4 and 5.

In claim 14, recite the limitation "a read operation" in line 2 and 5-6; "an evaluation phase" in line 3 and 5; "a pre-charge phase", in line 4-5;

"the read-select", in line 4 and "a read-select transistor", in line 5.

In claim 15, recite the limitation "a foot transistor", in line 17.

In claim 18, recite the limitation "a read operation" in line 2 and 9; "an evaluation phase" in line 3 and 8; "a pre-charge phase", in line 7;

"a read-select transistor", in line 5.

In claim 19, recite the limitation "an evaluation phase", in line 3.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Gannage et al, 5862099.

With regard to claim 1 and 7, Gannage discloses memory device comprising: a set of memory cells to store data, each memory cell comprising a read-pass transistor (fig. 2, 220), each read-pass transistor comprising a source and a gate that is HIGH if its corresponding memory cell stores a first logical state (fig. 2, corresponding to the output of node216, example: High logic) and is LOW if the corresponding memory cell stores a second logical state (fig.2, corresponding to the output of node 216, example Low logic); and a foot transistor (fig. 2, 202) comprising a drain connected to the source of one of the read-pass transistor , wherein the foot transistor is ON during a read operation on one of the memory cells (fig. 2, when colsel signal is high indication the transistor is being select state) and wherein the foot transistor is OFF when no read operation is performed on any of the memory cells (fig. 2, when colsel signal of transistor 202 is low, indication a non-select state).

With regard to claim 8, Gannage discloses a pullup pMOSFET (fig. 2, 218) to pull the bit line HIGH if ON, wherein the pullup pMOSFET is OFF during a read operation on one of the memory cells.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannage et al, No. 5862099 in view of Bernstein et al, Pat. No. 6404236.

With regard to claim 9, Gannage, as applied in prior rejection, disclosed all claimed subject matter except the memory device having an evaluation phase and a pre-charge phase such that a read operation is performed only during an evaluation phase, the memory device further comprising: a domino gate to turn OFF all the read-select transistors during a pre-charge phase, and during an evaluation phase to turn ON a read-select transistor if a read operation is performed on its memory cell. However, Bernstein discloses a memory logic device having an evaluation phase and a pre-charge phase such that a read operation is performed only during an evaluation phase, the memory device further comprising: a domino gate to turn OFF all the read-select transistors during a pre-charge phase, and during an evaluation phase to turn ON a read-select transistor if a read operation is performed on its memory cell (col. 2, line 35-col. 3, line 10) for the purpose of performing precharge and evaluation of a memory device. Therefore, it would have been obvious for one having an ordinary skill in the art

at the time the invention was made to utilized the logic circuit of Bernstein's to perform the two circuit function of precharge and evaluation operation in the configuration of the memory device of Gannage's so as to increase the speed of the memory device and the reliability and performance of the device (also with regard to claim 10).

Allowable Subject Matter

8. Claims 3-4 are allowed.

Claims 3-4 is considered allowable since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed inventions. Gannage et al and Bernstein et al taken individually or in combination, do not teach the claimed invention having limitation of a memory device having a read-access, read-pass and a foot transistor, wherein a subthreshold current of the read-access transistor flowing through the foot transistor causes the read-access transistor to be reverse biased if the memory cell stores the first logical state and the read-access transistor and the foot transistor are OFF and wherein a subthreshold current of the read-pass transistor flowing through the foot transistor causes the read-access transistor to be reverse biased if the memory cell stores the first logical state and the read-access transistor and the foot transistor are OFF.

8. Claim 11-15 and 18-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 16-17 and 20-21are allowed.

Claims 11-21 are considered allowable since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed inventions. Gannage et al and Bernstein et al taken individually or in combination, do not teach the claimed invention having limitation of the memory device includes a plurality of foot transistors in one-to-one correspondence with a subsets of memory cells, and that during a read operation on a particular memory cell belonging to a particular subset of the memory cells belonging to a particular set of memory cells, the foot transistor connected to that read-pass transistors in a the particular subset of memory cells is ON, where the foot transistor is OFF is connected to a subset of memory cells in which no read operation is performed. Prior art also does not discloses the memory device having memory cells grouped into 2 sub K subsets of memory cells so that there are 2 sub m+K memory cells is grouped into 2 sub K subsets of memory cells and a plurality of 2 sub m+k foot transistors in one-to-one correspondence with the 2 sub M+K subsets of memory cells and that wherein the foot transistor connected to the read-pass transistor in the particular subset of the memory cells is ON, where a foot transistor is OFF if connected to a subset of memory cells in which no read operation is performed.

Conclusion

9. Any inquiry concerning this communication should be directed to Connie Yoha whose telephone number is (703) 306-5731. The examiner can normally be reached on Monday-Thursday from 8:00 A.M. to 5:30 PM.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

C. Yoha

July 2003

Connie C. Yoha

Patent Examiner

Art Unit 2818